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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,589	08/30/2001	Rainald Sander	WMP-IFT631	1967

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LERNER AND GREENBERG, P.A.
PATENT ATTORNEYS AND ATTORNEYS AT LAW
Post Office Box 2480
Hollywood, FL 33022-2480

EXAMINER
PATEL, PARESH H

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,589	SANDER, RAINALD	
	Examin r	Art Unit	
	Paresh Patel	2829	

-- Th MAILING DATE of this communication app ars on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-28* is/are rejected.

7)☒ Claim(s) *29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: replace "current signal Us1" with --a current signal Is1--, "voltage signal Vs1" with --voltage signal Vs1-- and "current signal Us2" with --current signal Is2—throughout specification.

Appropriate correction is required.

Claim Objections

Claims 29-30 are objected to because of the following informalities: at line 6, "said comparator" should read --a comparator--.

Claim 22 is objected to because of the following informalities: at line 1, "claim 15" should read --claim 20--.

Claim 24 is objected to because of the following informalities: at line 3, "second" should read --first--.

Appropriate correction is required.

For the purpose of Examination and to expedite the process, Examiner considers above mention changes in claims 24 and 29-30. Also for claim 22, it is assumed that it depends from claim 20 instead claim 15.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 24-25 rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for **first evaluation circuit** includes a further resistor RS connected in series with said regulatable resistor T3, does not reasonably provide enablement for **second evaluation circuit** includes a further resistor RS connected in series with said regulatable resistor T3. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. **Second evaluation circuit** should read first evaluation circuit, which includes a further resistor connected in series with said regulatable resistor.

Claims 24-25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Regarding claim 24, the description of second evaluation circuit includes resistor R2 in series with T4 and not RS with T3, also first current signal is US1 and not U.

Claim 25 is rejected because it depends from rejected claim.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 22, 24-25 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 22, it is not clear how (e.g. in series or in parallel) first and second transistor are connected to each other and/or with current sensing transistor. It is also not clear how/why output signal of comparator drives these two transistors. Claim 22 also recites the limitation "said comparator" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 24, second evaluation circuit includes resistor R2 in series with T4 and not RS with T3 and hence it is indefinite.

Claim 25 is rejected because it depends from rejected claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Shibuya et al. (US 6140928).

Regarding claim 15, Applicant's admitted prior art (hereinafter APA) in fig. 1 discloses: a circuit configuration, comprising:

a load transistor [T1S];

a current sensing transistor [T2S] coupled to said load transistor;

a first evaluation circuit [Z2S];

APA lacks a second evaluation circuit; and a switch configuration including at least one switch for receiving a control signal and connecting said current sensing transistor to a selected evaluation circuit that is selected from the group consisting of said first evaluation circuit and said second evaluation circuit in dependence on said control signal.

Shibuya et al. (hereafter Shibuya) in fig. 2 discloses the use of second evaluation circuit [10 or 20 or 30] and the switch configuration [50] to select evaluation circuits. It would have been obvious to one having ordinary skill in the art at the time of the invention to use second evaluation circuit as taught by Shibuya with circuit configuration of APA to selectively evaluate/sence current or voltage.

Regarding claim 16, APA discloses: the circuit configuration according to claim 1, wherein: said load transistor has a load path [via Z1S] and a voltage across said load path [voltage between Vdd source of T1S]; and said switch [T3S] is driven depending on the voltage across said load path of said load transistor [using K1S].

Regarding claim 17, APA discloses: the circuit configuration according to claim 16, wherein: said current sensing transistor provides an output current [current through

T2S to Z2S]; and said switch configuration feeds the output current [I2] of said current sensing transistor to said selected evaluation circuit [Z2S].

Regarding claim 18, APA discloses: the circuit configuration according to claim 15, wherein: said current sensing transistor provides an output current [current through T2S to Z2S]; and said switch configuration feeds the output current [I2] of said current sensing transistor to said selected evaluation circuit [Z2S].

Regarding claim 19, APA discloses: the circuit configuration according to claim 15, comprising: a first chip having said load transistor and said current sensing transistor integrated therein [see lines 22-24 of page 2]; and a second chip having said switch configuration [see lines 22-24 of page 2], said first evaluation circuit integrated therein.

APA and Shibuya lacks said second evaluation circuit integrated in the second chip. It is obvious that the second evaluation circuit can also integrated in the second chip (as first evaluation circuit) for sensing the current when needed and for the same reason disclosed in rejection of claim 15.

Regarding claim 20, APA discloses: the circuit configuration according to claim 15, wherein: said load transistor has a load path [via T1S and Z1S] and a voltage across said load path [voltage between Vdd and source of T1S or voltage between source of T1S and ground]; said switch configuration has a comparator [K1S] configuration that receives a reference voltage [source voltage of T2S]; and said comparator configuration compares the voltage across said load path of said load transistor with the reference voltage [using K1S].

Regarding claim 21, APA discloses: the circuit configuration according to claim 20, wherein: said comparator configuration provides an output signal [output of K1S]; and said switch [T3S] is driven in dependence on the output signal of said comparator configuration.

Regarding claim 22, APA discloses: the circuit configuration according to claim ~~15~~ 20, wherein: said comparator configuration provides an output signal [output of K1S]; and said switch has a first transistor [T3S] and a second transistor [T3S] that are driven in dependence on the output signal of said comparator configuration.

Regarding claim 23, APA discloses: the circuit configuration according to claim 15, wherein: said first evaluation circuit includes a regulatable resistor [T3S] connected in series with said current sensing transistor [T2S]; and said first evaluation circuit includes a comparator configuration [K1S] regulating said regulatable resistor.

Regarding claim 24 as best understood by Examiner, APA discloses: the circuit configuration according to claim 23, wherein: said ~~second~~ first evaluation circuit includes a further resistor connected in series with said regulatable resistor; and a first current signal [signal between source terminal of T3S and terminal of Z2S] can be tapped off at said further resistor.

Regarding claim 25 as best understood by Examiner, APA discloses: the circuit configuration according to claim 24, wherein said regulatable resistor is designed as a transistor [T3S].

Regarding claim 26, APA discloses: the circuit configuration according to claim 23, wherein said regulatable resistor is designed as a transistor [T3S].

Regarding claim 27, APA discloses: the circuit configuration according to claim 15, wherein: said second evaluation circuit has a series circuit [T3S and Z2S can be used because one evaluation circuit is used to sense the current]; and said series circuit includes a resistor [Z2S] and a switch [T3S] connected in series with said current sensing transistor [T2S].

Regarding claim 28, Shibuya discloses said switch configuration has a switch position[inherent to 50, see fig. 5]; and said switch of said series circuit of said second evaluation circuit is driven in dependence on the switch position of said switch configuration.

Allowable Subject Matter

Claims 29 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Prior art does not teach or suggest a circuit configuration comprising: a switch having a first transistor and a second transistor being driven in dependence on the output signal of a comparator configuration; a first evaluation circuit including a regulatable resistor connected in series with a current sensing transistor; a second evaluation circuit; said first evaluation circuit including a comparator configuration regulating said regulatable resistor; said regulatable resistor including a control terminal;

and said first transistor including a load path connected between a terminal for receiving the supply potential and said control terminal of said regulatable resistor as further defined in claim 29.

Prior art does not teach or suggest a circuit configuration comprising: a switch having a first transistor and a second transistor being driven in dependence on the output signal of a comparator configuration; a first evaluation circuit; a second evaluation circuit including a series circuit; said series circuit including a resistor and a switch connected in series with said current sensing transistor; said switch of said series circuit including a control terminal; said second transistor including a load path connected between the supply potential and said control terminal of said switch of said series circuit as further define in claim 30.

Prior art to Baker (US 5874830) does not teach or suggest a switch having a first and second transistor to select a first or a second evaluation circuit as further defined in claims 29 and 30.

Prior art to Wrathall (US 4820968) does not teach or suggest a switch having a first and second transistor to select a first or a second evaluation circuit as further defined in claims 29 and 30.

Prior art to Ashley (US 5543632) does not teach or suggest a switch having a first and second transistor to select a first or a second evaluation circuit as further defined in claims 29 and 30.

Prior art to Castellucci et al. (US 5808508) does not teach or suggest a switch having a first and second transistor to select a first or a second evaluation circuit as further defined in claims 29 and 30.

Prior art to Chang et al. (US 6114844) does not teach or suggest a switch having a first and second transistor to select a first or a second evaluation circuit as further defined in claims 29 and 30.

Prior art to Yamatake (US 4560921) does not teach or suggest a switch having a first and second transistor to select a first or a second evaluation circuit as further defined in claims 29 and 30.

Prior art to Nakahara (US 6392392) does not teach or suggest a switch having a first and second transistor to select a first or a second evaluation circuit as further defined in claims 29 and 30.

Prior art to Carelli et al. (US 4789825) does not teach or suggest a switch having a first and second transistor to select a first or a second evaluation circuit as further defined in claims 29 and 30.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 703-306-5859. The examiner can normally be reached on M-F (8:30 to 4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703-308-1233. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Paresh Patel
June 6, 2003

Ernest T. Karlsen
ERNEST KARLSEN
PRIMARY EXAMINER